CLAIMS

I Claim:

1. A system comprising:

a serial flash memory; and

a programmable logic device having an interface coupled to the serial flash memory, wherein the interface is configured to identify the serial flash memory.

2. The system of Claim 1, wherein the serial flash memory operates in accordance with the serial peripheral interface (SPI) protocol.

3. The system of Claim 2, wherein the serial flash memory is coupled to the interface by a standard SPI four-wire interface.

4. The system of Claim 1, wherein the programmable logic device further comprises an address register configured to provide a start address to the serial flash memory, wherein the start address identifies an initial address to be accessed in the serial flash memory.

5. The system of Claim 4, further comprising means for initially setting the start address to a predetermined address.

6. The system of Claim 5, further comprising means for modifying the start address from the predetermined address to another address.

7. The system of Claim 1, further comprising means for updating a configuration of the programmable logic device stored in the serial flash memory during normal operation of the programmable logic device.

8. The system of Claim 1, wherein the programmable logic device is a field programmable gate array (FPGA).

9. A method of configuring a programmable logic device from a serial memory, the method comprising:

identifying a type of the serial memory with the programmable logic device;

selecting a read command in response to the type of the serial memory;

issuing the read command from the programmable logic device to the serial memory;

retrieving configuration data from the serial memory in response to the read command; and

configuring the programmable logic device in response to the retrieved configuration data.

10. The method of Claim 9, wherein the step of identifying the type of the serial memory comprises:

issuing a first read command from the programmable logic device to the serial memory;

determining that the serial memory is non-responsive to the first read command;

issuing a second read command, which is different than the first read command, from the programmable logic device to the serial memory;

determining that the serial memory is responsive to the second read command; and

identifying the type of the serial memory by the responsiveness of the serial memory to the second read command.

11. The method of Claim 9, wherein the step of identifying the type of the serial memory comprises:

applying control signals via one or more pins of the programmable logic device; and

identifying the type of the serial memory in

response to the control signals.

12. The method of Claim 9, wherein the step of issuing the read command from the programmable logic device to the serial memory comprises:

transmitting a read command from the programmable logic device to the serial memory; and

transmitting a start address from the programmable logic device to the serial memory.

13. The method of Claim 12, wherein the step of issuing the read command from the programmable logic device to the serial memory further comprises transmitting one or more dummy bytes from the programmable logic device to the serial memory.

14. The method of Claim 12, further comprising initializing the start address in the programmable logic device when the programmable logic device is powered on.

15. The method of Claim 14, further comprising modifying the start address in the programmable logic device to a second start address after the programmable logic device is configured.

16. The method of Claim 15, further comprising:

issuing a second read command from the programmable logic device to the serial memory, wherein the second read command includes the second start address;

retrieving a second set of configuration data from the serial memory in response to the second read command, starting at the second start address; and

reconfiguring the programmable logic device in response to the second set of configuration data.

17. The method of Claim 9, wherein the step of retrieving the configuration data from the serial memory is performed as a continuous read operation.

18. The method of Claim 9, wherein the serial memory is a standard peripheral interface (SPI) flash memory.

19. A method of configuring a programmable logic device from a serial memory, the method comprising:

sequentially issuing a plurality of different read commands from the programmable logic device to the serial memory;

determining which read command causes the serial memory to respond; and

identifying the serial memory from the read command that results in a response from the serial memory.